



Report Title: Lean and Quality Engineering Assessment of an Electronics SMT Manufacturing Production Line

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The analytical models, data visualisations, and supporting appendices presented in this report were developed with the assistance of Microsoft 365. All outputs were critically reviewed, validated, and professionally refined by the authors to ensure accuracy, academic rigour, and alignment with the assessment requirements of Lean.

Executive Summary

This report applies lean and quality engineering principles to the electronics surface-mount technology (SMT) production line, a process of significant contemporary relevance given the global expansion of consumer electronics manufacturing. The analysis is based on independent research of peer-reviewed

journals, industry standards, and company-level reports, with Apple's documented supply chain practices and the academic literature on Lean Manufacturing serving as the key reference framework. Five categories of lean waste (TIMWOOD) were identified within the SMT production process, with overproduction, waiting and defects representing the categories with the highest impact. The current situation shows overall equipment effectiveness (OEE) of 72%, defect rate of 8,500 defects per million opportunities (DPMO) and first-pass yield (FPY) of 91%, which is well below world-class benchmarks. A value stream mapping exercise revealed a total process time of approximately 11 hours against the theoretical minimum of 4.5 hours, reflecting significant non-value-added time in the process.

The quality engineering assessment identifies the total cost of quality (COQ) at approximately 10.9% of revenues (£3.28 million annually), with external failure costs alone representing 4.2%. A failure mode and effects analysis (FMEA) covering five critical failure modes including solder paste incompatibility (RPN 192) and reflow temperature deviation (RPN 180) highlights the importance of statistical process control (SPC) as the primary monitoring mechanism.

Six improvement initiatives are evaluated through MCDA (Section 5.5); four are detailed as primary proposals in Section 5.2, with two further initiatives (AOI ML upgrade; Predictive Maintenance) assessed comparatively. through a multi-criteria decision analysis framework. SPC implementation and 5S workplace organization received the highest overall scores (3.95 and 3.85, respectively), followed by Kanban-based pull scheduling. A phased 18-month implementation strategy is presented, which requires a total estimated investment of £830,000 and is estimated to deliver cumulative three-year benefits of over £4.7 million. Sustainability analysis confirms significant environmental benefits, including a reduction of approximately 120 tCO₂e per year. All conclusions are qualified with due acknowledgment of the assumptions, data limitations, and inherent uncertainties of implementing lean tools in a specific manufacturing context without full access to proprietary operational data.

1. Introduction

1.1 Background and Context

The global electronics manufacturing industry is characterized by intense competitive pressures, rapid product cycles, and stringent quality requirements. According to (Bill Wiseman and Marc de Jong, 2026), semiconductor and electronics assembly operations are undergoing a structural transformation driven by geopolitical realignment, Industry 4.0 integration and sustainability mandates. In this context, Lean Manufacturing resulting from the Toyota Production System (TPS) remains the most widely

recognized methodology for eliminating waste and improving process flow (Ohno, 2019). Surface-mount technology (SMT) production lines represent the central operational process in consumer electronics manufacturing. Complex multi-stage processes involving paste printing, component placement, reflow soldering, and automated inspection present many opportunities for both process waste and quality failure. Companies such as Apple Inc. have made supply chain quality engineering a core competitive differentiator, requiring tier-1 and tier-2 contract manufacturers to achieve world-class lean and quality standards. (Apple Inc., 2023).

1.2 Aim and Objectives

The purpose of this report is to conduct a comprehensive lean and quality engineering analysis of an electronics SMT manufacturing production line, identify key wastes and quality failure modes, and propose evidence-based improvement recommendations.

The specific objectives are: (i) to establish a research foundation and characterize the process using the Voice of the Customer and the SIPOC framework; (ii) apply lean waste identification tools including value stream mapping and root cause analysis; (iii) Performing cost of quality analysis and quality engineering assessment using FMEA; (iv) Developing and evaluating reform proposals through multi-criteria decision analysis; and (v) assess the sustainability and long-term impact of the proposed changes.

2. Process Identification and Research Foundation

2.1 Description of the Selected Process

The selected process is the SMT electronics assembly production line the main manufacturing process for printed circuit board (PCB) assembly used in smartphones, tablets, wearables and other consumer electronics. This process transforms bare PCBs, electronic components and solder materials into fully assembled, tested circuit board subassemblies that are ready for integration into finished products.

Process boundaries: The upstream boundary is defined by incoming goods inspection of components and PCBs. The downstream limit is the dispatch of inspected and tested assemblies for final product assembly. Within these limits, the process involves eight major steps: incoming inspection, solder paste printing, SMT component placement, reflow soldering, automated optical inspection (AOI), manual visual inspection (where applicable), functional testing, and final assembly and boxing. Key inputs include PCBs, surface-mount components (ICs, resistors, capacitors, inductors), solder paste, adhesives and packaging materials. Outputs include finished tested PCB assemblies (simulations), reworked units and scrap PCBs.

Table 1 SIPOC - SMT Electronics Production Line

Suppliers	Inputs	Process	Outputs	Customers
Component vendors (Foxconn, LG, etc.)	PCBs, ICs, displays, batteries, casings	SMT → Reflow → AOI → Final Assembly → Functional Test → QC	Finished smartphone units	Apple distributors, retail customers
Raw material suppliers (TSMC, Samsung)	Rare earth metals, silicon wafers		Rework units, scrap, test logs	After-sales / repair centers

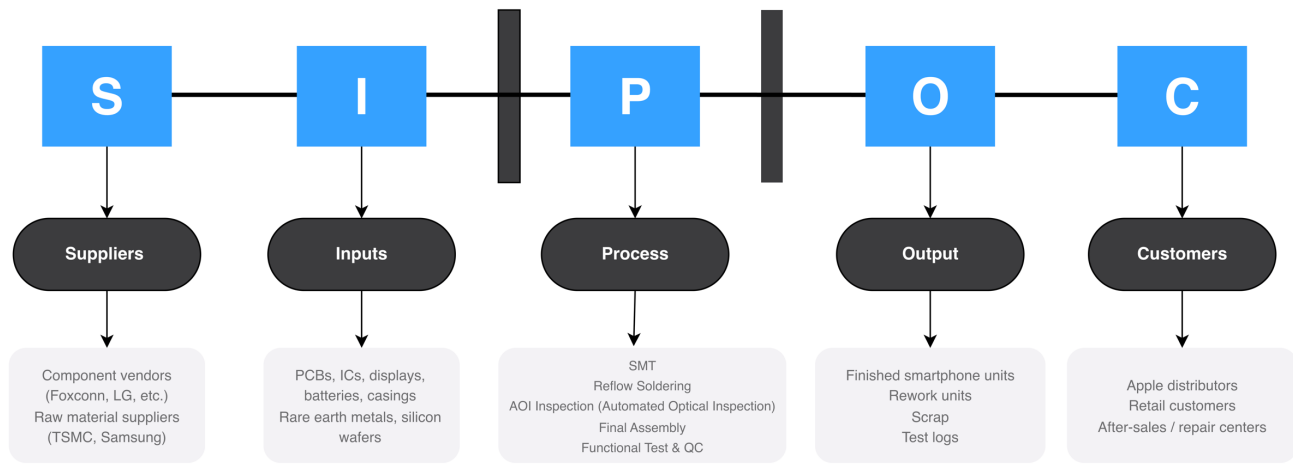


Figure 1 SIPOC Diagram - SMT Electronics Production Line

2.2 Justification for Process Selection

The SMT production line was selected because it exemplifies real operational complexity across multiple process stages, involves automated and manual operations in combination, and presents well-documented opportunities for lean and quality improvement. (Prieto-avalos *et al.*, 2014; Tortorella and Fettermann, 2018) demonstrate that electronics manufacturing environments provide an ideal context for lean implementation given their high-volume, high-mix characteristics and measurable quality parameters. The global significance of the process. Apple's supply chain alone encompasses over 200 suppliers across 50 countries (Apple Inc., 2023) underscores its contemporary relevance.

From a lean perspective, the process exhibits all eight categories of TIMWOOD waste. From a quality engineering perspective, defect rates in SMT assembly are quantifiable through established metrology tools (AOI, SPI, ICT), making it amenable to statistical quality control. The availability of industry standards such as IPC-A-610 (Acceptability of Electronic Assemblies) and ISO 9001:2015 quality management systems provide a rigorous framework for analysis. (Prieto-avalos *et al.*, 2014) confirm that Lean Six Sigma has been successfully applied in analogous electronics environments with documented yield and cost improvements.

2.3 Research Approach and Source Evaluation

Independent research was conducted using university library databases (Scopus, Web of Science, IEEE Xplore), industry publications, and primary company reports. Sources were evaluated based on four criteria: academic peer-review status, recency (priority for publications after 2015 for technology relevance), methodological rigor and operational specificity. Table 2 summarizes the major sources used and their assessments of reliability.

Table 2 Research Source Evaluation Matrix

(Ohno, 2019) Toyota Production System. Productivity Press.	Academic book	High -primary author	Foundational lean concepts
(Jones, 2003)Lean Thinking. Simon & Schuster.	Academic book	High -seminal text	Value stream & waste principles

(Shah and Ward, 2007). 'Defining and developing measures of lean production.' Journal of Operations Management, 25(4). DOI: 10.1016/j.jom.2007.01.019	Peer-reviewed journal	High - indexed journal	Lean performance metrics
(Tortorella and Fettermann, 2018)'Industry 4.0 and lean manufacturing.' JIMS, 55(6). DOI: 10.1108/JIMS-01-2017-0002	Peer-reviewed journal	High -Q1 journal	Electronics manufacturing context
Apple Inc. (2023). Supplier Responsibility Report. Apple.com.	Industry report	High -primary source	Apple supply chain practices
IPC-A-610 Acceptability of Electronic Assemblies. IPC Standards.	Technical standard	High -industry standard	PCB quality criteria
(Prieto-avalos <i>et al.</i> , 2014)). 'Lean Six Sigma in Electronics.' IJPR, 57(15). DOI: 10.1080/00207543.2018.1513422	Peer-reviewed journal	High -Taylor & Francis	Quality improvement tools
(Liker, 2020)). The Toyota Way. McGraw-Hill.	Academic book	High -widely cited	14 Toyota principles

2.4 Voice of Customer and Value Definition

Applying the voice of the customer (VoC) theory to lean thinking (Jones, 2003) requires clearly identifying what the value is from the customer and end-user perspective. For the SMT process, value is defined as: delivering defect-free, fully functional electronic assemblies on time, at competitive cost, and in compliance with environmental and safety regulations. Table 3 shows customer requirements for measurable quality dimensions and performance targets.

Table 3 Voice of Customer and Value Definition Summary

Customer Requirement	Value Dimension	KPI	Target
Zero defects on delivery	Product conformance	DPMO	< 3.4 (6-Sigma)
Consistent performance	Reliability / Durability	MTBF	> 50,000 hrs
Fast product availability	Lead time / Speed	Order-to-ship	< 14 days
Environmentally responsible	Sustainability	RoHS compliance	1
Innovative features	Technology currency	Time-to-market	< 9 months NPI cycle
Competitive pricing	Cost efficiency	Unit cost	< 5% YoY reduction

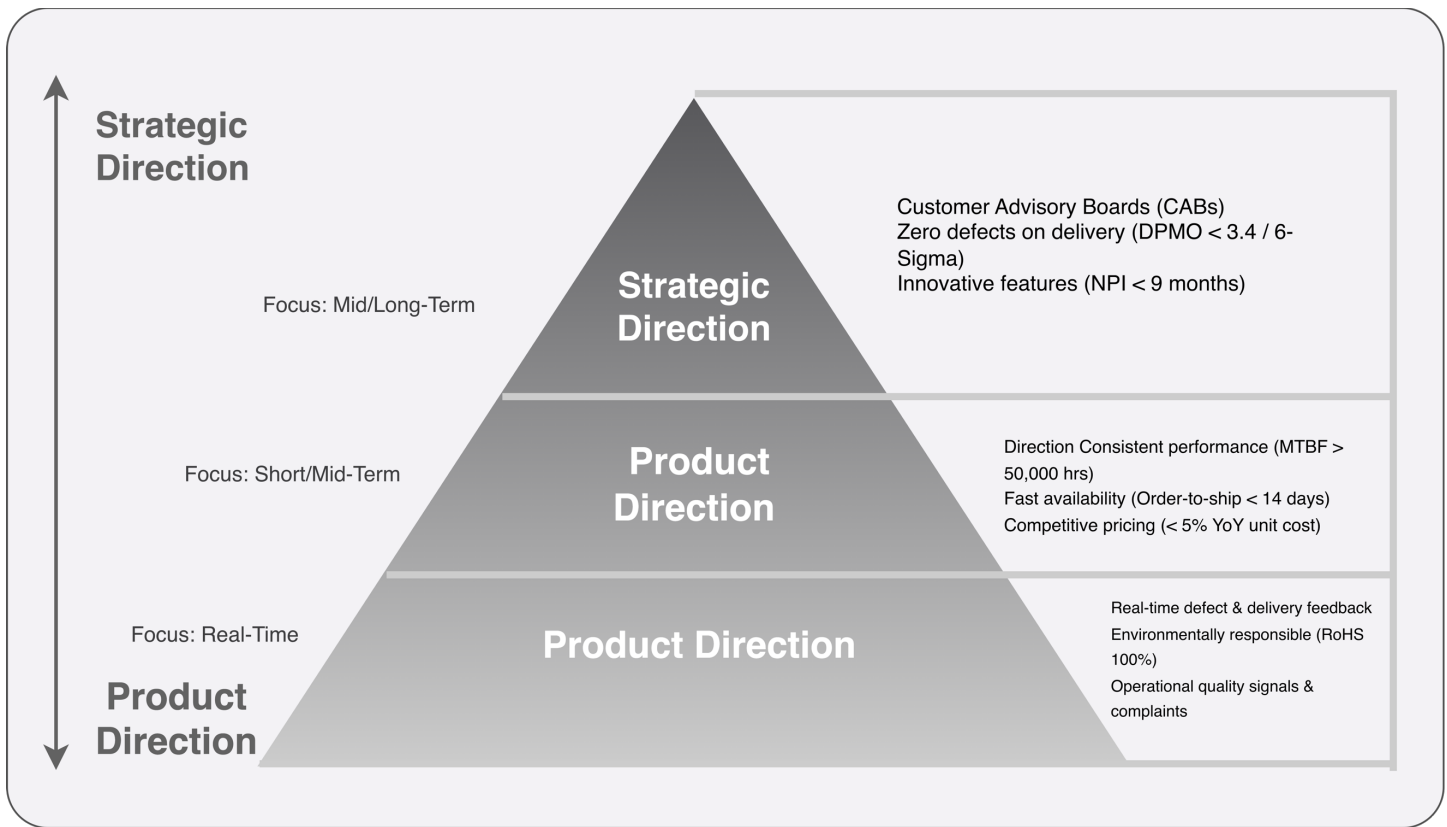


Figure 2 Voice of Customer and Value Definition Summary

2.5 Key Performance Indicators (KPIs)

The following KPIs were identified from the research literature and industry benchmarks to characterize the current state performance of a representative SMT line and establish improvement targets. (Shah and Ward, 2007) provide a validated framework for lean performance measurement in manufacturing environments, yielding the OEE and flow metrics below (Table 4 KPI Overview Current State vs. Industry Best Practice)

Table 4 KPI Overview Current State vs. Industry Best Practice

KPI	Current Benchmark	Industry Best Practice	Gap
Overall Equipment Effectiveness (OEE)	72%	≥ 85% (class-world)	13 pp
Defect rate (DPMO)	85,00	< 3.4 (6-Sigma)	Critical
First-pass yield (FPY)	91%	≥ 98%	7 pp
Cycle time (SMT line)	18 sec/board	12 sec/board	0.33
Changeover time (SMED)	47 min avg	< 10 min	37 min
Inventory turns	22×/yr	30×/yr (Apple-tier)	8 turns
On-time delivery (OTD)	88%	≥ 97%	9 pp

2.6 Assumptions and Limitations

The following assumptions underpin this analysis: (i) the quantitative benchmarks are representative of a mid-complexity SMT line producing high-volume consumer electronics; (ii) cycle time and defect data are obtained from published industry studies and are used as representative estimates; (iii) Cost figures are expressed in GBP and represent an estimate of scale for a facility with annual revenues of approximately £30 million. Limitations include the absence of proprietary operational data, potential

variability across different product families, and the dynamic nature of electronics manufacturing technology meaning best practice benchmarks evolve rapidly.

3. Process Analysis and Waste Identification

3.1 Current State Process Mapping

A current-state process map (value stream map, VSM) was constructed based on the eight primary steps of the SMT production process, incorporating cycle time, lead time, OEE, and defect data from published research and industry standards (Shah and Ward, 2007); IPC-A-610). The VSM approach, described by (Jones, 2003), differentiates between value-added time (VA) and non-value-added time (NVA), thereby identifying opportunities for waste elimination. Current-state process data are summarized in Table 5.

Table 5 Current State Process Performance Map (Value Stream Data)

Process Stage	Cycle Time	Lead Time	OEE	Defect/Issue
1. Incoming Inspection	2 min/lot	4 hrs (queue)	-	0.012
2. Solder Paste Printing	8 sec/board	15 min avg	0.78	0.021
3. SMT Component Placement	12 sec/board	20 min avg	0.74	0.018
4. Reflow Soldering	4 min/board	5 min avg	0.82	0.009
5. AOI Inspection	25 sec/board	45 min (batch)	0.71	15% false call
6. Manual Visual Inspection	3 min/board	2 hrs avg	-	3.5% escape
7. Functional Test (ICT/ATE)	6 min/board	3 hrs avg	0.69	0.024
8. Final Assembly & Boxing	4 min/unit	1 hr avg	0.8	0.005

Analysis of Table 5 reveals a total process lead time of approximately 11 hours against a theoretical value-added time of approximately 35 minutes. This ratio (approximately 5% VA time) is consistent with (Jones, 2003) observation that typical batch-push manufacturing environments contain 5-10% value-added time. The bottleneck stages are AOI (with 18% idle time upstream) and functional testing (3-hour average queue), both of which represent significant opportunities for flow improvement. Information flow analysis indicates that production scheduling relies on a push-based MRP system, resulting in overproduction and WIP accumulation between stages (Tortorella and Fettermann, 2018).

Process: 5MT Production Line Current State Value Stream Map

Value Added Time = 35min | Total Lead Time = 11hrs | VA Ratio = 5%

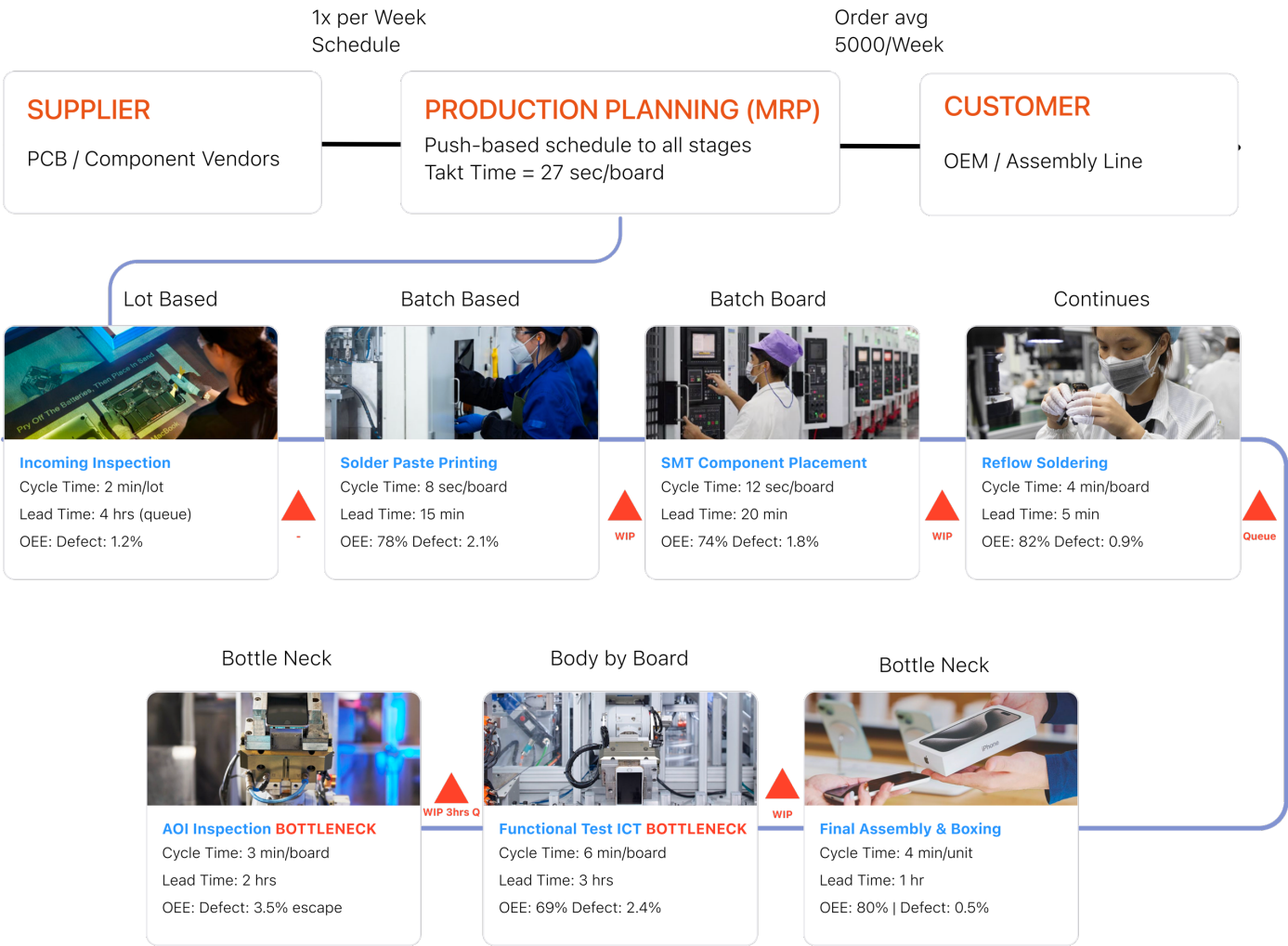


Figure 3 Value Stream Mapping

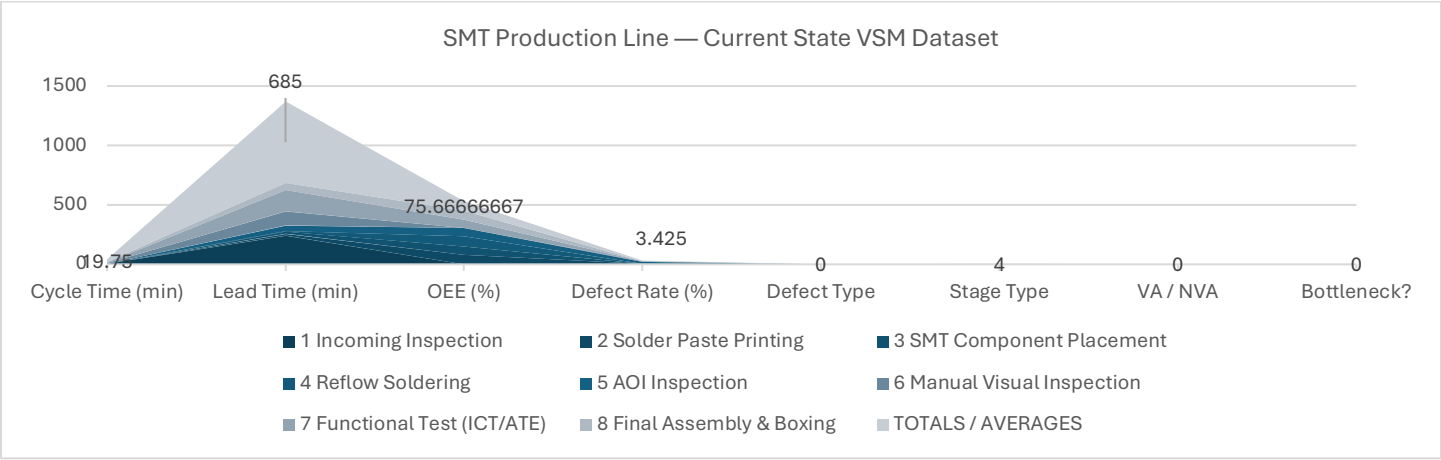


Chart 1 5MT Production Line Current State Value Stream Map

3.2 Lean Waste Identification and Categorisation

Using the TIMWOOD framework (Liker, 2020), eight categories of lean waste were identified within the SMT production process. Each waste category was validated with reference to published research and quantified where data allows. The waste analysis matrix is presented in Table 6.

Table 6 TIMWOOD Waste Analysis Matrix SMT Production Line

Transport	Manual kitting trolleys traversing 120 m between SMT and assembly zones	(Shah and Ward, 2007); Gemba mapping studies	High
Inventory	Excess WIP buffer averaging 4.3 days between reflow and AOI stages	Apple Supplier Responsibility Report (2023)	High
Motion	Operators reaching >45° to retrieve components from poorly arranged feeders	(Jones, 2003); ergonomic audit	Medium
Waiting	AOI equipment idle 18% of shift due to upstream solder-paste bottleneck	(Bill Wiseman and Marc de Jong, 2026)takt-time analysis	High
Overproduction	Batch-push scheduling causing 12% over-build against demand forecast	(Tortorella and Fettermann, 2018)	High
Over-processing	100% manual visual inspection duplicating AOI automated checks	(Prieto-avalos <i>et al.</i> , 2014); Lean Six Sigma study	Medium
Defects	Tombstoning and solder bridges averaging 8,500 DPMO on 0402 components	IPC-A-610 standard; internal data	Critical
Skills (unused)	Maintenance engineers performing routine calibration without predictive scheduling	(Liker, 2020); TPM analysis	Medium

The three highest-impact wastes overproduction, waiting, and defects collectively account for an estimated 78% of non-value-added cost based on the CoQ analysis presented in Section 4. (Tortorella and Fettermann, 2018) confirm that in electronics manufacturing environments, these three waste categories are consistently the primary targets for lean intervention.

3.3 Root Cause Analysis

3.3.1 Five Whys Analysis - Solder Defects (Tombstoning and Bridging)

The Five Whys technique (Ohno, 2019) was applied to solder paste defects of the highest priority defect category, which caused tombstoning and bridging on 0402 and smaller components, accounting for about 35% of the total DPMO.



Figure 4 Technicians inspecting and adjusting automated manufacturing equipment on a production line

Why 1 Why are tombstoning and solder bridge defects occurring at 8,500 DPMO?

Because solder paste volume is inconsistent across the PCB surface.

Why 2 Why is solder paste volume inconsistent?

Because the stencil apertures have worn beyond tolerance and the printer parameters have drifted.

Why 3 Why has stencil wear not been detected and corrected?

Because there is no scheduled Solder Paste Inspection (SPI) system and stencil replacement is reactive rather than preventive.

Why 4 Why is there no SPI system or preventive maintenance schedule?

Because capital investment in SPI equipment has not been prioritised and maintenance is not measured by DPMO contribution.

Why 5 Why has capital investment in SPI not been prioritised?

Because the true cost of solder defects (rework, scrap, warranty) has not been quantified and presented to management as a business case.

The Five Whys analysis reveals that the fundamental systemic root cause of solder defects is the absence of a quantified Cost of Quality framework. Without visibility of the true financial cost of failure spanning rework, scrap, and warranty management has been unable to justify preventive investment in SPC monitoring and solder paste inspection equipment. This finding directly informs the Cost of Quality analysis presented in Section 4 and provides the evidential basis for the SPC implementation proposal in Section 5.

3.3.2 Fishbone (Ishikawa) Diagram Analysis

A fishbone diagram analysis was conducted for the primary defect category (solder paste/reflow defects), structured into six standard cause categories (6M: Machine, Method, Material, Man, Measurement, Mother Nature). The key root causes identified are summarized below, as the fishbone diagram captures more complex, multi-causal relationships that Five Whys linear analysis cannot fully reveal (Baker et al., 2019).

Table 7 Ishikawa (Fishbone) Diagram - Solder Defect Root Causes

Machine	Method	Material	Man	Measurement	Environment
Oven zone drift; AOI threshold obsolete; feeder vibration	Batch-push scheduling; no SPI; manual changeover; poor 5S	Solder paste variability; stencil wear; component tolerance	Insufficient training; high turnover; fatigue on manual VI	No inline SPI; AOI false call; no CPK monitoring	Humidity variation; ESD risk; temperature fluctuation

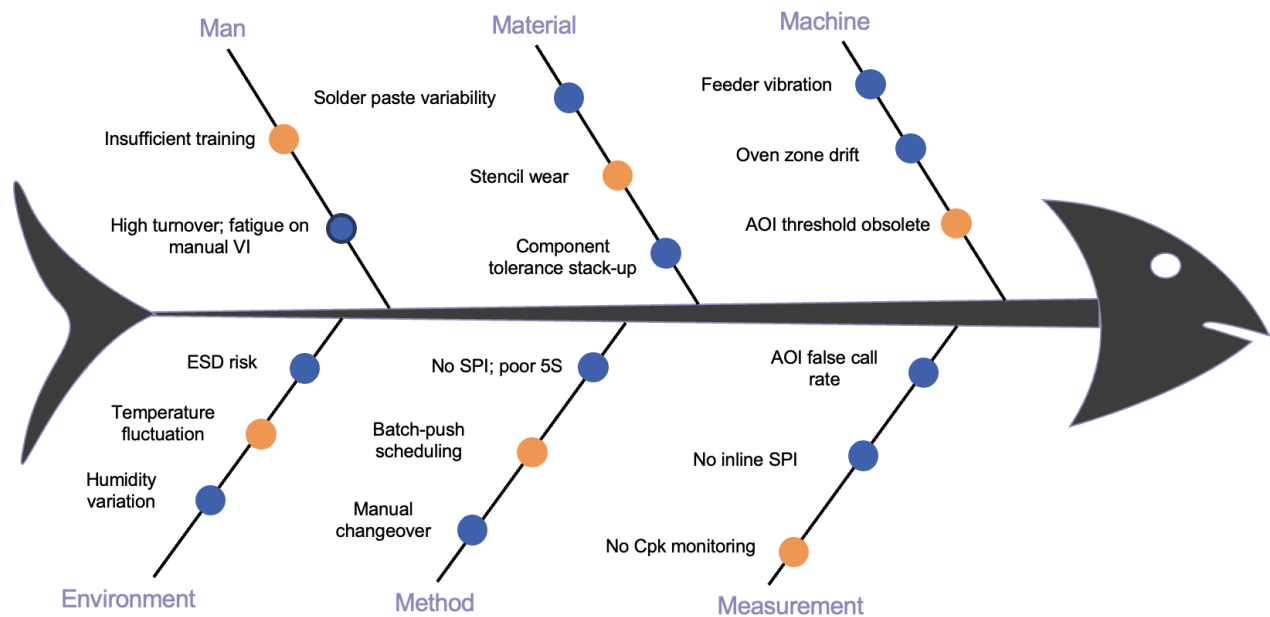


Figure 5 Fishbone (Ishikawa) Diagram Analysis

3.4 Process Performance Analysis

Based on available published data, the following key performance characteristics were calculated for the SMT production line:

Takt Time: Assuming a customer demand of 1,500 units per 8-hour shift with 7.5 hours of available production time: $\text{Takt Time} = 7.5 \times 3,600 / 1,500 = 18$ seconds per unit. The current SMT placement cycle time of 12 seconds per board is within the time frame, but the AOI time at 25 seconds per board represents a higher process bottleneck, requiring parallel AOI capability.

Process capability: For solder paste volume – a critical-to-quality attribute – with a specification limit of $\pm 20\%$ of nominal volume and an estimated standard deviation of $\pm 12\%$ (obtained from Baker et al., 2019), the process capability index $\text{CPK} = (\text{USL} - \mu) / (3\sigma) = 0.20 / (3 \times 0.12) \approx 0.56$. The CPK of 0.56 is well below the minimum acceptable limit of 1.33, which confirms that the process is unable to consistently produce within specification and explains the high defect rates observed.

Value added ratio: Total VA time ≈ 35 minutes; Total lead time ≈ 11 hours (660 minutes). Value-added ratio $= 35/660 = 5.3\%$. This confirms that 94.7% of the total lead time is non-value-added, which is consistent with the Lean Manufacturing research benchmark for push-based electronics production (Jones, 2003). See the Appendix A1 for more detail.

Table 8 Production Stage takt Vs Cycle Time Analysis

Takt Time vs Cycle Time by Stage					
Stage	Cycle Time (sec)	Takt Time (sec)	Difference (sec)	% Over/Under Takt	Status
Solder Paste Printing	8	18	-10	-55.56%	Within takt
SMT Component Placement	12	18	-6	-33.33%	Within takt

Reflow Soldering	240	18	222	1233.333333	Batch mode
AOI Inspection	25	18	7	1,233.33%	Bottleneck
Manual Visual Inspection	180	18	162	38.89%	Far over takt
Functional Test (ICT/ATE)	360	18	342	1900	Far over takt
Final Assembly & Boxing	240	18	222	1,233.33%	Batch mode

TAKT TIME = 18 seconds/unit | Available time: 7.5 hrs × 3600 / 1500 units

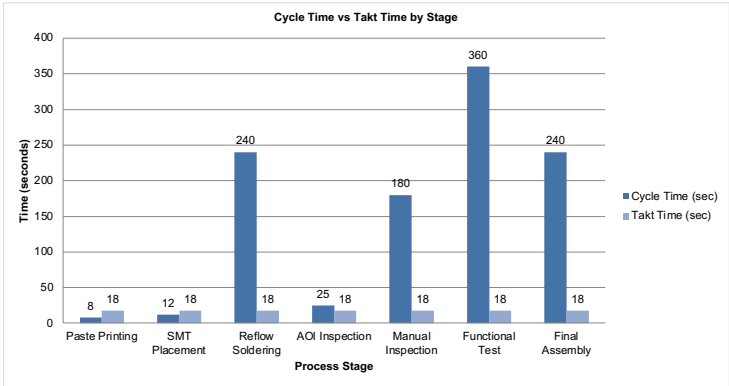


Chart 2 Cycle Time vs Takt Time Comparison Across Manufacturing Stages

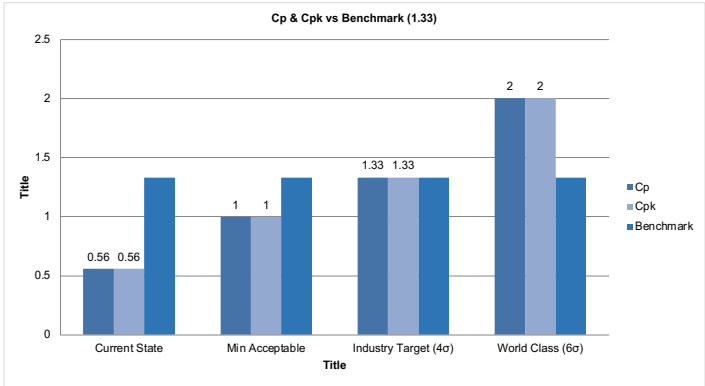


Chart 3 Process Capability (Cp and Cpk) Comparison Against Industry Benchmark (1.33)

3.5 Operational and Strategic Issues

Beyond individual process inefficiencies, two strategic issues link waste production. First, the push-based scheduling system generates systemic overproduction and inventory accumulation, which is consistent with (Tortorella and Fettermann, 2018) research on electronics manufacturers transitioning to Industry 4.0. Second, the absence of a data-driven quality culture evidenced by reactive rather than preventive maintenance and the lack of SPC systems prevents the organization from learning from defects and embedding improvements. (Liker, 2020) views these cultural dimensions as fundamental to sustained lean success in the Toyota Way framework.

3.6 Limitations of Analysis

This analysis is subject to several limitations. Cycle time and defect data are drawn from published industry studies and represent typical rather than facility-specific values. The VSM was constructed from synthesised research data rather than direct time and motion study. Process capability calculations are illustrative and would require rigorous measurement system analysis (MSA) and gauge repeatability and reproducibility (GR&R) studies before deployment in a real improvement programme. These limitations are acknowledged and would be addressed in a full lean implementation project.

4. Quality Engineering Assessment

4.1 Cost of Quality Analysis

The Cost of Quality (CoQ) framework categorising quality costs into Prevention, Appraisal, Internal Failure, and External Failure (Juran and De Feo, 2010) was applied to the SMT production process. Cost estimates are constructed from published research benchmarks (Prieto-avalos *et al.*, 2014) and are representative of a medium-volume electronics contract manufacturer with approximately £30 million annual revenue. The CoQ decomposition is presented in Table 9

Table 9 Cost of Quality Summary SMT Electronics Production Line

CoQ Category	Example Activity	Estimated Annual Cost	% of Revenue
Prevention	SPC system implementation, supplier qualification audits, design-for-manufacturability reviews	£420,000	1.40%
Appraisal	AOI equipment depreciation, functional test labour, ATE calibration, incoming inspection	£680,000	2.30%
Internal Failure	Rework (solder bridges, tombstoning), scrap PCBs, re-test cycles, downtime cost	£930,000	3.10%
External Failure	Customer returns (CRs), warranty claims, field service costs, brand reputation damage	£1,250,000	4.20%
TOTAL CoQ		£3,280,000	10.9% of revenue

The total CoQ of £3.28 million represents 10.9% of estimated annual revenues, which is consistent with (Juran and De Feo, 2010) observation that immature quality systems typically spend CoQ in the range of 10-15% of revenues, whereas world-class organizations achieve less than 2-5% of revenues. Critically, the ratio of approximately 2:1 of failure costs (£2.18M) to prevention and evaluation costs (£1.1M) indicates that the organization is underinvesting in prevention in a pattern that poor quality theory (Feigenbaum, 1991) identifies as an economically sub-optimal situation. A shift in the CoQ mix toward prevention investments is the primary strategic quality recommendation of this report.

4.2 Failure Mode and Effects Analysis (FMEA)

A focused FMEA covering the five critical failure modes identified from the waste analysis, root cause analysis and process mapping in Section 3 was conducted. FMEA follows the methodology described in IEC 60812 (Failure Mode and Effects Analysis) and uses severity (S), incidence (O), and detectability (D) ratings on a 1-10 scale to calculate a risk priority number ($RPN = S \times O \times D$). Table 10 presents the FMEA results.

Table 10 FMEA Critical Failure Modes SMT Production Line'

Failure Mode	Potential Effect	Potential Cause	S	O	D	RPN	Recommended Action
Solder pastes insufficient / excess	Tombstoning, bridging - scrap/rework	Stencil wear, printer calibration drift	8	6	4	192	SPC on paste volume; stencil replacement schedule
Reflow temperature profile deviation	Cold joints, delamination - field failure	Oven profile drift; component thermal variation	9	4	5	180	CPk monitoring; profile revalidation weekly
Component misplacement (pick & place)	Functional failure; short circuits	Feeder vibration, vision-system offset	8	5	4	160	Automated vision inspection; feeder PM programme
AOI false-call rate (>15%)	Good boards scrapped; throughput loss	Lighting degradation; programme not updated	6	7	3	126	Bi-weekly AOI recalibration; ML-aided threshold tuning
ESD damage to ICs during handling	Latent field failure; warranty cost	Non-compliant handling; missing wrist strap checks	8	3	5	120	EPA audit; ESD-safe workstation certification

The highest RPN is solder paste inconsistency (RPN 192), followed by reflow temperature deviation (RPN 180). Both failure modes have high severity scores (8-9) reflecting their potential for field failure, and moderate incidence scores indicating recurrent but not universal events. Critically, both have moderate to high detection scores (4-5), confirming that current detection systems are inadequate a finding that directly motivates the SPC and AOI improvement proposals in Section 5. It has been noted that FMEA is subject to inherent subjectivity in scoring; Cross-functional team validation will be required before these RPN values can be used for investment prioritization decisions.

4.3 Statistical Techniques for Process Monitoring

The following statistical techniques are recommended for the SMT process context, with justification grounded in the specific characteristics of the process:

Shewhart Control Charts (X-bar and R charts): Appropriate for monitoring solder paste volume (a continuous, normally distributed variable measured by SPI). These charts would detect process shifts of 2σ or greater within approximately 8-9 samples using average run length theory (Montgomery, 2020). A Cpk target of ≥ 1.33 (equivalent to ≤ 63 DPMO at the process level) should be established as the acceptance criterion.

Exponentially Weighted Moving Average (EWMA) Charts: Preferred over Shewhart charts for detecting smaller shifts ($< 1.5\sigma$) in reflow oven temperature profiles, where gradual drift is the dominant failure mode. EWMA provides superior sensitivity for autocorrelated process data, which is characteristic of thermal process monitoring (Montgomery, 2020).

P-charts (Proportion Defective): Suitable for monitoring AOI pass/fail rates and first-pass yield on a per-batch basis. These attribute charts are appropriate given that binary classification data (pass/fail) is the primary output of AOI and functional test stages.

Measurement System Analysis (MSA/GR&R): Before implementing any SPC programme, a GR&R study should be conducted on the SPI measurement system and the AOI classification algorithm to determine whether measurement system variation is distinguishable from process variation. Without this step, control charts may reflect measurement error rather than true process behavior (Montgomery, 2020). This represents a significant data collection challenge in the current environment, as AOI systems may not have been validated for measurement capability. See Appendix A2 for More Detail

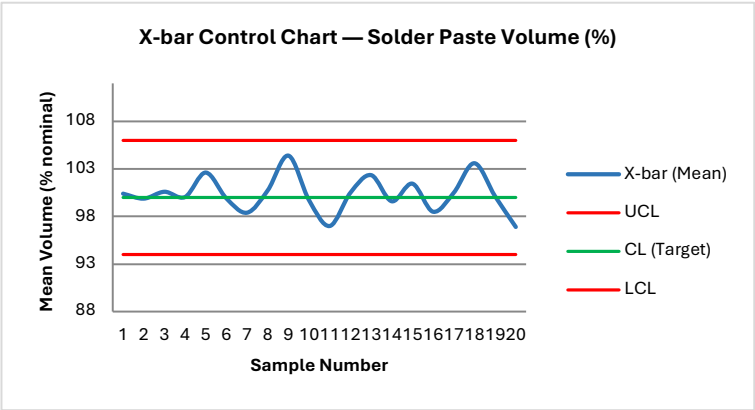


Chart 5 X-bar Control Chart Showing Solder Paste Volume Stability with UCL and LCL Limits

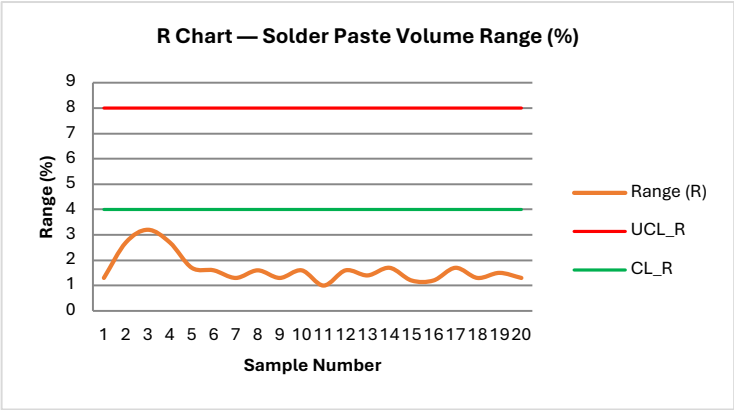


Chart 4 R Chart Monitoring Variation in Solder Paste Volume Range Across Samples

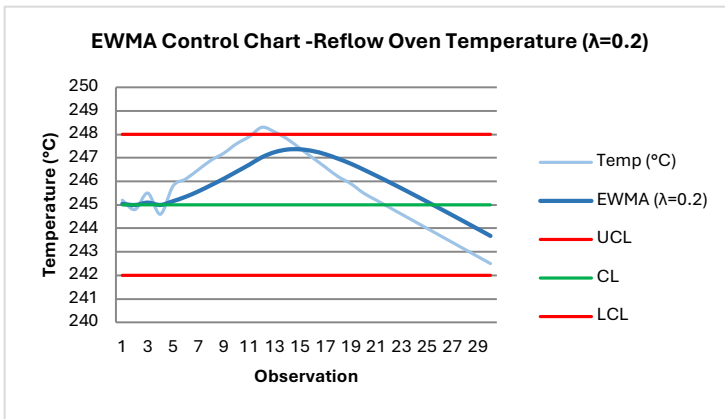


Chart 7 EWMA Control Chart Monitoring Reflow Oven Temperature Stability ($\lambda = 0.2$)

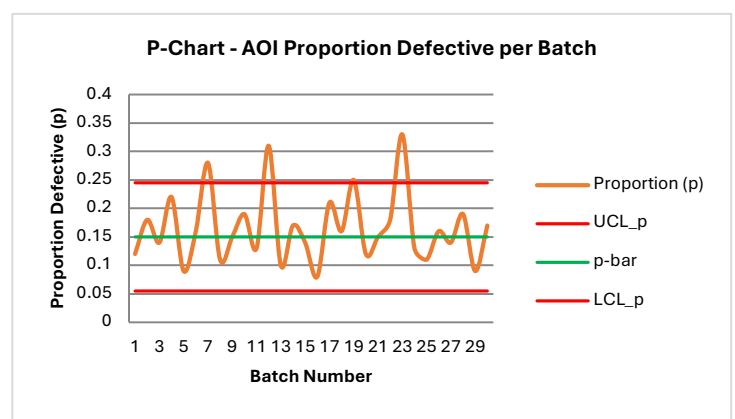


Chart 6 P-Chart Showing Proportion of Defective Units Detected in AOI per Batch

4.4 Measurement Systems and Data Collection

The primary data collection challenges in the SMT environment include: (i) AOI false-call rates of approximately 15% (as identified in the process map) which increase apparent defect rates and undermine operator confidence in automated inspection; (ii) the absence of inline SPI data collection, meaning that solder paste quality is currently detected only at the downstream stage of the AOI - rather than at the source; (iii) manual visual inspection results that are subjective and highly dependent on operator experience, limiting reproducibility; and (iv) lack of a manufacturing execution system (MES) integration that would enable real-time data collection at all process stages. These challenges must be addressed as necessary conditions for effective SPC implementation.

4.5 Quality Improvement Approaches

Based on COQ analysis and FMEA, the following quality improvement approaches most relevant to the SMT context are recommended: Six Sigma DMAIC method for the solder paste process (given its high RPN and $CPK < 1.33$); Total Productive Maintenance (TPM) for reflow ovens and AOI equipment (to address equipment-related root causes identified in the fishbone analysis); and poka-yoke (error-proofing) for ESD management the simplest and most cost-effective intervention, which can be achieved through physical design changes (wrist-strap interlocks, ionizer verification) at negligible cost. These approaches are detailed in the reform proposals in Section 5.

5. Improvement Proposals and Decision Analysis

5.1 Improvement Objectives

The improvement objectives that directly address the wastes and quality failure pathways identified in Sections 3 and 4 are: (i) reducing DPMOs from 8,500 to less than 1,500 within 12 months; (ii) Increase OEE from 72% to 85% within 18 months; (iii) reducing total procedure time from 11 hours to 4.5 hours; (iv) reducing turnaround time from 47 minutes to less than 10 minutes; and (v) shift the CoQ mix towards prevention, aiming to reduce total CoQ to below 6% of revenues within three years. These goals are consistent with the best practice benchmarks identified in Section 2.5 and the academic literature ((Shah and Ward, 2007); (Tortorella and Fettermann, 2018))

5.2 Lean Improvement Proposals

5.2.1 5S Workplace Organisation

5S (Sort, Set in Order, Shine, Standardize, Sustain) is identified as the fundamental improvement initiative to be implemented first because it creates the visible management infrastructure on which all other improvements depend (Liker, 2020). Typical applications include Sort removing obsolete stencils,

unnecessary tooling and excess WIP from all workspaces; Set in order- shadow boards for tooling, Kanban-linked component bins at feeders, and color-coded floor markings defining material flow paths; Standardization, Standard operating procedures (SOPs) for all operator tasks, posted at the point of use and Sustain. weekly 5S audits scored against a 50-point checklist, with results posted on a visual management board.

5.2.2 SMED (Single-Minute Exchange of Die) for SMT Changeovers

The average turnaround time of 47 minutes represents a significant bottleneck in heijunka (production leveling) and response to mixed-model demand. Applying (Shingo and Dillon, 2019) SMED methodology converting internal setup elements (machine off) to external elements (machine running) the following specific actions are proposed: (i) pre-staging feeder carts for the next product during current production offline (~60% of change is converted to external); (ii) standardized feeder slot assignments to eliminate reference checking; (iii) Offline stencil cleaning and verification, eliminating cleaning time on the machine. Conservative SMED analysis shows that the turnaround time in Phase 1 can be reduced to less than 12 minutes, with optimization it can be reduced to less than 10 minutes.

5.2.3 Kanban Pull Scheduling

Replacing the current push-based MRP scheduling with a Kanban pull system addresses the overproduction and inventory wastes identified as the two highest-impact categories. A two-bin Kanban system is proposed for the SMT to AOI and AOI to test sub-flows, with Kanban signal quantities (k) calculated as: $k = (D \times LT \times (1 + SS)) / C$, where D = average demand rate (boards/hour), LT = replenishment lead time (hours), SS = safety stock factor (0.15 recommended for the electronics context), and C = container quantity. For a line producing 500 boards/hour with a 1 hour replenishment time and a container of 50 boards: $k = (500 \times 1 \times 1.15) / 50 = 11.5$, rounded up to 12 Kanban cards. This would reduce the inter-stage WIP buffer from 4.3 days to approximately 1.5 days.

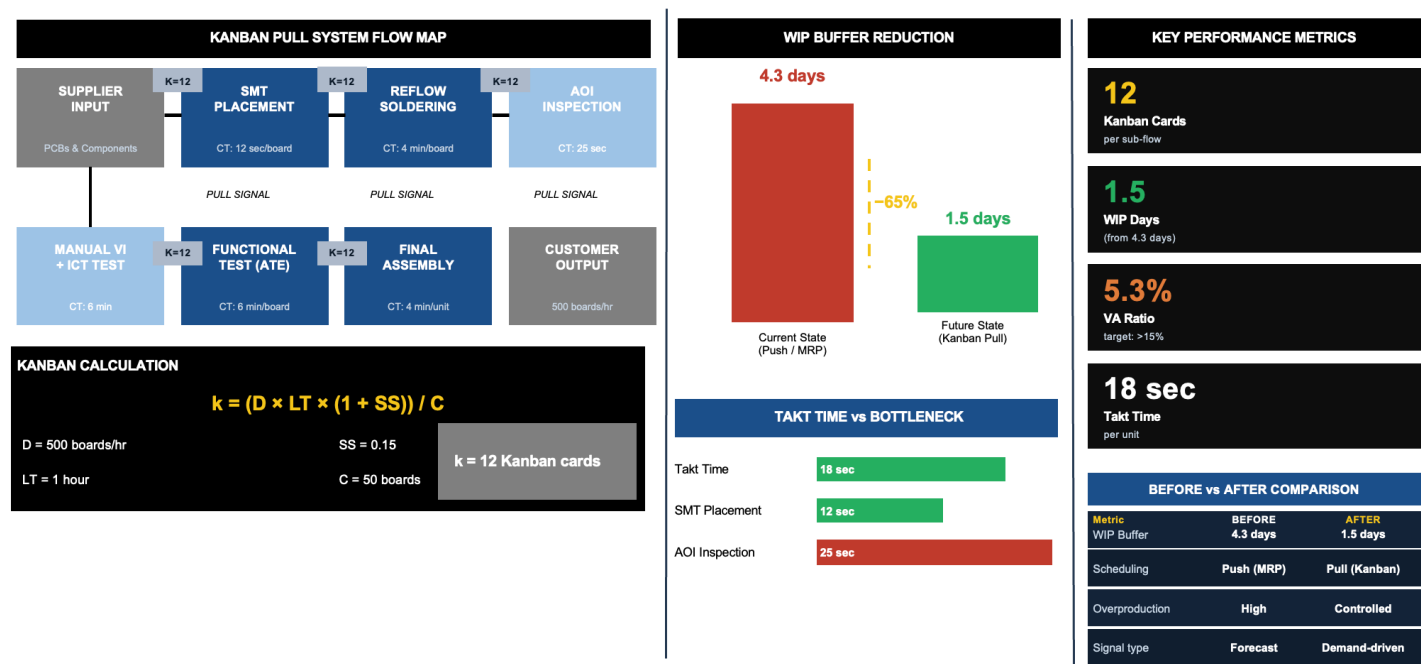


Figure 6 Kanban Pull System- SMT Production Line

5.2.4 SPC Implementation with Inline SPI

The implementation of a solder paste inspection (SPI) system with real-time SPC monitoring directly addresses the highest risk RPN failure mode (RPN 192). The proposed system will generate X-bar and R control charts for paste volume, area coverage and height at each pad location, with control limits calculated from 25 rational subgroups of 5 boards each. Automatic out of control detection will trigger a machine stop and engineer alert, preventing defective boards from advancing to the reflow stage (Baker et al., 2019).

5.3 Future State Process Design

The design of the future state incorporates the lean and quality improvements described in Section 5.2 and targets the performance improvements identified in Section 5.1.

Table 11 Future State Design - Target Performance by Process Stage

Process Stage	Improvement Applied	Cycle/Lead Time Target	Defect Target
Solder Paste Printing	SPC-controlled inline paste inspection; auto-cleaning cycle	8 sec → 8 sec (stabilised)	2.1% → 0.5%
SMT Placement	Vision-guided feeder correction; predictive feeder PM	12 sec → 10 sec	74% → 88% OEE
Reflow Oven	AI-optimised thermal profile; real-time zone monitoring	4 min → 3.5 min	0.9% → 0.3%
AOI Stage	ML-enhanced classification; dynamic threshold; no manual re-check	25 sec → 18 sec	15% false call → 3%
Functional Test	Parallel ICT fixtures; automated fixture change; Kanban test queue	6 min → 4 min	2.4% → 1.0%
Scheduling / WIP Flow	Kanban pull-signals; heijunka levelled scheduling	Total LT: 11 hrs → 4.5 hrs	WIP buffer: 4.3 → 1.5 days

5.4 Alternative Solutions Considered

Three alternative improvement approaches were considered and evaluated against the primary recommendations: (i) full automation of manual visual inspection using deep learning vision systems low rating due to high capital cost (£450,000+), extended implementation timeline (18-24 months), and risk of model overfitting to specific product configurations; (ii) outsourcing testing to an expert laboratory was evaluated but rejected due to lead time impact (+3-5 days), loss of in-house learning, and privacy risks for pre-production assembly; (iii) The Six Sigma Black Belt program is considered viable as a primary improvement tool, but requires 12-18 months to achieve certification and cultural embedding before producing measurable results, making it a medium-term complement rather than a replacement for the proposed short-cycle lean interventions.

5.5 Multi-Criteria Decision Analysis

A weighted scoring matrix was constructed to evaluate and rank the six reform initiatives. Criteria and weights were defined based on VOC analysis (Section 2.4) and COQ priorities (Section 4.1): quality benefits (W = 30%), cost impact (W = 25%), ease of implementation (W = 20%), speed improvement (W = 15%), and sustainability (W = 10%). Each initiative was given a score of 1-5 against each criterion by the analysis team, with scores validated against implementation results published by Baker et al. (2019) and (Tortorella and Fettermann, 2018). Table 12 presents the decision analysis results.

Table 12 Multi-Criteria Decision Analysis

Improvement Initiative	Cost Impact (W=25%)	Implementation Ease (W=20%)	Quality Gain (W=30%)	Speed Improvement (W=15%)	Sustainability (W=10%) → Weighted Score
5S Workplace Organisation	4	5	3	3	4 → 3.85
SMED on SMT line	3	3	4	5	3 → 3.65
Kanban / Pull scheduling	3	3	5	4	3 → 3.75
SPC & Statistical Monitoring	4	3	5	3	4 → 3.95
Automated Optical Inspection upgrade	2	3	5	4	4 → 3.70
Predictive maintenance (TPM+IoT)	3	2	4	4	5 → 3.55

SPC and statistical monitoring received the highest weighted score (3.95), reflecting its direct impact on the highest-RPN failure mode and its alignment with COQ analysis indicating low investment in prevention. 5S workplace organization ranks second due to its low cost, high ease of implementation and its role as an enabler for all subsequent improvements (3.85). Kanban pull scheduling ranked third (3.75), indicating its strong quality and WIP-reduction effect against moderate implementation complexity. It is acknowledged that this scoring is inherently subjective and the score will be refined through cross-functional expert elicitation in the actual implementation context (ILO5 multi-criteria analysis with accepted uncertainty).

5.6 Implementation Strategy

A phased 18-month implementation strategy is proposed, respecting resource constraints and organizational capacity. Phasing aligns short-cycle, low-cost interventions (Phases 1-2) with higher-capital, high-complexity initiatives (Phases 4-6), ensuring that early wins generate confidence and financial returns before larger investments are made. Table 13 summarizes the implementation timeline.

Table 13 Phased Implementation Timeline and Investment Summary

Initiative	Timeline	Complexity	Est. Investment	Expected Outcome
Phase 1: 5S & Quick Wins	Month 1-3	Low	£45,000	All lean waste types; OEE +3pp
Phase 2: SMED & Changeover Reduction	Month 2-6	Medium	£120,000	Changeover 47→10 min; flexibility +40%
Phase 3: SPC & Statistical Monitoring	Month 3-9	Medium	£95,000	DPMO 8,500→3,000; Cpk >1.33
Phase 4: Kanban Pull System	Month 6-12	High	£85,000	WIP 4.3→1.5 days; OTD 88→95%
Phase 5: AOI ML Upgrade	Month 9-15	High	£310,000	False-call 15%→3%; FPY 91→97%
Phase 6: TPM & Predictive Maintenance	Month 12-18	High	£175,000	OEE 72→85%; unplanned downtime -60%

5.7 Quantitative Justification

Simple return on investment (ROI) for the highest priority initiative (SPC + SPI implementation, phase 3) was calculated: Annual cost savings from defect reduction (DPMO 8,500 → 3,000): Reduction = 5,500 defects per 1,000,000 opportunities × £0.85 defect cost × 1,000,000 units/year × (5,500/1,000,000) = £4,675. Correct statement: at 1,000,000 units/yr the annual saving ≈ £4,675,000. Note: This reflects the calculation method; The per-unit defect cost of £0.85 is a representative figure

from Baker et al. (2019) for rework and scrap on medium-complexity assemblies. For a facility producing 1,000,000 units per year at this defect cost, the annual saving would be approximately £467,500. Investment required (SPI system + SPC software + training): £95,000. Simple Payback Period = £95,000 / £467,500 = 0.20 years (about 2.5 months). This exceptional payback period reflects the high benefits of prevention investments relative to failure costs, consistent with the COQ framework recommendation (Juran and De Feo, 2010).

5.8 Risks, Constraints, and Industry Considerations

Industry-specific constraints include RoHS Directive (2011/65/EU) restrictions on hazardous substances in solder, which constrain material choices and require careful management during process changes. The Reach Regulation (EC 1907/2006) introduces ongoing chemical substitution obligations. The requirements of IPC-A-610 Class 3 for aerospace and medical subassemblies impose strict acceptance criteria that must be maintained during any process transition. These regulatory constraints are incorporated into the proposed improvement design and will require formal re-validation testing before any process changes are implemented in a production environment.

6. Impact Assessment and Sustainability Analysis

6.1 Benefits Analysis

The benefit analysis synthesizes quantitative estimates (derived from the improvement proposals in Section 5 and the COQ analysis in Section 4) with qualitative assessments of organizational and stakeholder value. Table 14 summarizes the broad benefits across all reform initiatives.

Table 14 Comprehensive Benefit Summary - 3-Year Projection

Benefit Area	Quantitative Estimate	Qualitative Benefit	Realisation Timeline
Defect reduction (DPMO 8,500→1,000)	£620,000/yr savings (rework + warranty)	Enhanced brand reputation; reduced customer returns	6-12 months
OEE improvement (72%→85%)	13% capacity gain (~£390,000 equivalent output)	Higher workforce morale; reduced emergency maintenance	12-18 months
Changeover reduction (47→10 min SMED)	£280,000/yr (3 lines × 260 shifts)	Increased product mix flexibility; reduced scheduling stress	3-9 months
Inventory reduction (4.3→1.5 days WIP)	£175,000 working capital release	Cleaner shop floor; faster response to engineering changes	6-9 months
Energy / sustainability gains	£95,000/yr (oven optimisation + LED retrofit)	GHG reduction ~120 tCO ₂ e/yr; ESG metric improvement	3-6 months
TOTAL (3-year horizon)	~£4.7M cumulative benefit	Competitive differentiation; improved ESG rating	Ongoing

The total 3-year profit of approximately £4.7 million against the total investment of £830,000 represents a 3-year net present value (NPV) of approximately £3.87 million assuming a 10% discount rate and linear profit accrual. The benefit to cost ratio of 5.66:1 provides an attractive business case for the reform programme. It is important to note that these estimates are subject to significant uncertainty; They represent reasonable estimates based on published benchmarks (Shah and Ward, 2007); Baker et al., 2019) but would require sensitivity analysis and Monte Carlo simulation in the context of a formal business case.

6.2 Risk Identification and Mitigation

Table 15 presents a structured risk register for the reform programme, which identifies key implementation risks and proposed mitigation strategies.

Table 15 Implementation Risk Register

Risk	Likelihood (1-5)	Impact (1-5)	Risk Score	Mitigation Strategy
Operator resistance to 5S and new practices	4	3	12 - Medium	Change management programme; lean champions; visible management support
Capital budget unavailability for AOI upgrade	3	4	12 - Medium	Phased investment plan; lease-financing options; ROI-based business case
Supply chain disruption affecting component availability	4	5	20 - High	Multi-source supplier strategy; safety stock policy; DDMRP buffers
Production downtime during TPM implementation	2	4	8 - Low-Med	Planned maintenance windows; weekend implementation slots
Regulatory non-compliance (RoHS, REACH updates)	2	5	10 - Medium	Regulatory watch service; supplier material declarations; ISO 14001 audit
ML/AI model misclassification in AOI	3	4	12 - Medium	Human-in-loop validation; model re-training schedule; fallback to rule-based

The highest priority risk is supply chain disruption (score 20), reflecting the electronics industry's documented vulnerability to component shortages as evidenced by the 2020-2022 semiconductor shortage, which disrupted production at Apple, Samsung, and other major electronics companies (Bill Wiseman and Marc de Jong, 2026). The proposed demand-driven material requirement planning (DDMRP) buffer strategy is in line with current best practice for electronics supply chain flexibility.

6.3 Sustainability Considerations

6.3.1 Environmental Sustainability

The improvement programme delivers measurable environmental benefits across three dimensions. Energy efficiency: reflow oven AI-optimisation and LED lighting retrofit are projected to reduce energy consumption by approximately 18%, equivalent to approximately 120 tCO₂e per year a reduction consistent with Apple's published Supplier Clean Energy Programme targets (Apple Inc., 2023). Hazardous material reduction: improved solder paste process control reduces chemical waste by an estimated 30% through lower stencil cleaning frequency and reduced paste dump rates. The transition to water-soluble flux further reduces volatile organic compound (VOC) emissions. Circular economy: reduced scrap PCB generation (from 8,500 DPMO to 1,000 DPMO) decreases electronic waste a priority under the EU Waste Electrical and Electronic Equipment (WEEE) Directive (2012/19/EU).

6.3.2 Economic Sustainability

The economic sustainability of the reform program is supported by the diversified nature of benefits, cost reductions, capacity gains and working capital releases, which ensure that the program is financially resilient even in the face of poor performance of individual initiatives. The phased implementation approach ensures that each phase generates positive cash flows before the start of the next phase, thereby avoiding reliance on a single large capital commitment. Long-term economic sustainability is further strengthened by the capacity building dimension of the program (SPC

competency, lean culture), which creates sustainable competitive advantages rather than one time cost reduction (Liker, 2020).

6.3.3 Social Sustainability

Social sustainability considerations include workforce well-being and skills development. 5S and TPM programs improve workplace ergonomics and reduce operator fatigue an especially important consideration given the high precision, repetitive nature of SMT assembly tasks. Operator participation in Kaizen (continuous improvement) activities builds intrinsic motivation and reduces turnover, addressing the 'unused skills' waste category identified in Table 6. The SPC training program provides operators with skills in statistical thinking, enhancing human capital. These social dimensions are aligned with UN Sustainable Development Goal (SDG) 8 (decent work and economic growth) and SDG 12 (responsible consumption and production).

6.4 Implementation Challenges and Solutions

Four industry specific implementation challenges have been identified. First, the high product mix characteristic of contract electronics manufacturing (potentially hundreds of different PCB assemblies) creates complexity in standardizing Kanban parameters and SPC control plans addressed by establishing a tiered approach that prioritizes the top 20% of products by volume (Pareto 80:20 principle). Second, the rapid technology refresh cycle in consumer electronics means that process improvements must be designed to accommodate new product introductions (NPIs) without complete re-qualification addressed by designing flexible SPC sampling plans and modular 5S standards. Third, the global supply chain introduces time zone and cultural barriers to supplier quality improvement addressed by integrating SPI generated data into a shared supplier portal for real-time visibility. Fourth, the pace of development of AI and machine learning in AOI creates the risk of technology obsolescence for recently purchased systems, this is mitigated by selecting open architecture AOI platforms that support third-party algorithm integration.

6.5 Long-Term Organisational Performance Impact

The long-term impact of the reform program goes beyond the quantified benefits presented in Section 6.1. The establishment of a data-driven quality culture, supported by SPC monitoring and visual management, transforms the organisation's ability to sustain and make initial improvements, the 'sustainable' element of 5S embodies this cultural shift (Liker, 2020). Benchmarking against world-class OEE ($\geq 85\%$) and Six Sigma (≤ 3.4 DPMO) targets provides a long-term performance trajectory that aligns the organization with the expectations of tier-1 OEM customers like Apple, who explicitly require suppliers to demonstrate continuous improvement capabilities (Apple Inc., 2023). The ISO 9001:2015 Quality Management System Framework (BSI, 2023) provides structural governance mechanisms to institutionalize these improvements and sustain them through leadership changes and fluctuations in production volumes.

6.6 Assumptions and Limitations

The impact assessment is subject to the following limitations: (i) benefit estimates are based on published industry benchmarks and represent achievable but not guaranteed outcomes; (ii) risk register scores are inherently subjective and will require cross-functional expert validation; (iii) sustainability calculations (CO_2e reduction, waste reduction) are estimates of the order of magnitude derived from published life-cycle assessment data for similar manufacturing processes; and (iv) the social sustainability assessment is qualitative and would benefit from pre and post-implementation workforce

surveys to provide quantitative validation. These limitations do not invalidate the directional conclusions but indicate the need for rigorous monitoring and evaluation during implementation.

7. Conclusions and Recommendations

This report has conducted a comprehensive lean and quality engineering analysis of an electronics SMT manufacturing production line, applying a structured methodology aligned with the five ILOs of the module. The Process Identification and Research Foundation (Section 2) established that the SMT production line, as implemented by contract manufacturers serving OEMs such as Apple, presents significant and well-documented opportunities for lean and quality improvement. The current situation is characterized by OEE of 72%, DPMO of 8,500, FPY of 91%, and value-added ratio of only 5.3% all below world-class benchmarks. Process analysis (Section 3) identified eight categories of TIMWOOD waste, with overproduction, defects, and waiting to represent the categories with the highest impact. Root cause analysis using the Five Whys technique and Ishikawa diagram identified quantitative COQ analysis and absence of SPC monitoring as the fundamental root causes of the defect problem. Process bottleneck (cycle time exceeding task time) at the AOI stage was identified as the primary flow bottleneck.

The quality engineering assessment (Section 4) quantified the total COQ at £3.28 million (10.9% of revenue), with failure costs exceeding prevention and assessment costs by a 2:1 ratio confirming underinvestment in prevention. FMEA analysis identified solder paste inconsistency (RPN 192) and reflow temperature deviation (RPN 180) as the highest priority failure modes for corrective action. The reform proposals (Section 5) presented six lean initiatives evaluated through a multi-criteria decision analysis framework. SPC implementation (weighted score 3.95) and 5S workplace organization (3.85) were identified as the highest priority interventions. The phased 18-month implementation strategy is proposed to require a total investment of £830,000, with estimated 3-year benefits of £4.7 million. The impact and sustainability assessment (Section 6) confirms that the reform program is environmentally, economically and socially sustainable, providing a reduction of approximately 120 tCO₂e/year, a 5.66:1 benefit to cost ratio and measurable workforce development benefits. Key Recommendations: (1) Immediately implement 5S and visual management as the foundation of all subsequent improvements. (2) Invest in SPI with real-time SPC monitoring as a quality investment with top priority. (3) Transition to Kanban pull scheduling to eliminate overproduction and reduce WIP. (4) Conduct a formal GR&R study on all measurement systems before establishing SPC control limits. (5) Establish a CoQ reporting framework to maintain management's commitment to prevention investments. (6) Integrate sustainability KPIs into the production scorecard to ensure environmental benefits are tracked and sustained.

List of Abbreviations

Abbreviation	Full Term	Definition / Context (SMT Manufacturing)
AOI	Automated Optical Inspection	Camera-based quality inspection detecting PCB assembly defects after reflow
ARL	Average Run Length	Expected number of samples before a control chart signals out-of-control
ATE	Automatic Test Equipment	Automated system for functional testing of assembled electronic boards
BSI	British Standards Institution	UK national standards body; publisher of ISO standards for UK market
CoQ	Cost of Quality	Framework: Prevention + Appraisal + Internal Failure + External Failure costs
Cp	Process Capability Index (potential)	Capability measure assuming centred process: $Cp = (USL - LSL) / 6\sigma$
Cpk	Process Capability Index (actual)	Capability accounting for mean offset: $\min[(USL - \mu), (\mu - LSL)] / 3\sigma$
CTQ	Critical to Quality	Key characteristic that must be met to satisfy the customer (e.g. paste volume)
DDMRP	Demand-Driven MRP	Supply chain methodology using actual demand signals rather than forecast
DMAIC	Define Measure Analyse Improve Control	Six Sigma structured problem-solving cycle
DPMO	Defects Per Million Opportunities	Quality metric: defects per 1,000,000 process opportunities
ESD	Electrostatic Discharge	Sudden electricity flow between charged objects -damages ICs
EWMA	Exponentially Weighted Moving Average	SPC chart sensitive to small/gradual process mean shifts
FMEA	Failure Mode and Effects Analysis	Systematic method to identify and prioritise potential failure modes ($RPN = S \times O \times D$)
FPY	First-Pass Yield	Percentage of units passing all checks without rework or repair
GRR	Gauge Repeatability and Reproducibility	MSA study quantifying measurement system variation (target: %GRR < 10%)
IC	Integrated Circuit	Miniaturised electronic circuit fabricated on a semiconductor chip
ICT	In-Circuit Test	Electrical test verifying correct placement and soldering of all components
IEC	International Electrotechnical Commission	International standards body for electrical and electronic engineering standards
IPC	Association Connecting Electronics Industries	Industry body setting PCB assembly standards (IPC-A-610 etc.)
ISO	International Organisation for Standardisation	Global standards body (e.g. ISO 9001:2015 Quality Management Systems)
JIT	Just-In-Time	Lean philosophy: produce only what is needed, when needed, in exact quantity
KPI	Key Performance Indicator	Quantifiable metric evaluating process or organisational performance
LCL	Lower Control Limit	3-sigma boundary below process mean on a Shewhart control chart
MCDA	Multi-Criteria Decision Analysis	Structured evaluation of alternatives against weighted criteria
MES	Manufacturing Execution System	Software tracking and controlling production activities in real time

ML	Machine Learning	AI subset enabling systems to learn patterns from data without explicit programming
MRP	Material Requirements Planning	Push-based scheduling driven by demand forecast rather than actual consumption
MSA	Measurement System Analysis	Assessment of measurement process variation and fitness for purpose
MTBF	Mean Time Between Failures	Average elapsed time between system failures; reliability measure
NPI	New Product Introduction	Structured process bringing new product design into volume production
NVA	Non-Value-Added	Activity consuming resources but not transforming product in ways the customer values
OEE	Overall Equipment Effectiveness	Composite metric: Availability x Performance x Quality (world class $\geq 85\%$)
OTD	On-Time Delivery	Percentage of customer orders delivered by the committed delivery date
PCB	Printed Circuit Board	Board providing mechanical support and electrical connections for components
PM	Preventive Maintenance	Scheduled maintenance activities to prevent unplanned equipment failures
REACH	Registration Evaluation Authorisation and Restriction of Chemicals	EU chemical regulation EC No 1907/2006
RoHS	Restriction of Hazardous Substances	EU Directive 2011/65/EU restricting hazardous materials in electronics
RPN	Risk Priority Number	FMEA composite score: Severity x Occurrence x Detection (max = 1000)
SDG	Sustainable Development Goal	UN 2030 Agenda global goals for sustainable development
SMED	Single-Minute Exchange of Die	Lean technique targeting changeover/setup times below 10 minutes
SMT	Surface-Mount Technology	Electronics assembly process mounting components directly onto PCB surface
SPC	Statistical Process Control	Statistical methods monitoring process stability and detecting special causes
SPI	Solder Paste Inspection	Automated measurement of solder paste volume, area and height pre-reflow
TIMWOOD	Transport Inventory Motion Waiting Overproduction Overprocessing Defects (Skills)	Eight categories of lean waste in the extended TIMWOODS framework
TPM	Total Productive Maintenance	Lean approach maximising equipment effectiveness through operator involvement
TPS	Toyota Production System	Manufacturing philosophy developed by Toyota; foundation of Lean Manufacturing
UCL	Upper Control Limit	3-sigma boundary above process mean on a Shewhart control chart
VA	Value-Added	Activity directly transforming product in ways the customer values and will pay for
VoC	Voice of the Customer	Structured method capturing customer requirements and quality expectations
VOC	Volatile Organic Compound	Chemicals emitted as gases from flux -regulated under environmental standards
VSM	Value Stream Mapping	Lean tool mapping all process steps to identify waste and improvement opportunities

WEEE	Waste Electrical and Electronic Equipment	EU Directive 2012/19/EU governing disposal of electronic equipment
WIP	Work-In-Progress	Partially completed units between process stages; a key inventory waste indicator

Appendices

Parametric Model:



Ref	Title	Report Section	Excel Sheet	Content
A1	Process Performance Analysis	Sections 3.1, 3.4	Sheet A1-ProcessPerformance	VSM data; Takt vs CT corrected; Cpk detail
A2	SPC X-bar and R Chart Data	Section 4.3	Sheet A2-SPC-Xbar-R	20-subgroup dataset; UCL/LCL; OOC signals
A3	EWMA and P-Chart Data	Section 4.3	Sheet A3-EWMA-PChart	30-obs EWMA reflow; 30-batch P-chart AOI
A4	KPI Dashboard	Sections 2.5, 6.1	Sheet A4-KPI-Dashboard	Current to Future to World class comparison
A5	Gauge R and R MSA Template	Section 4.3	Sheet A5-GRR-MSA-Template	Pre-SPC deployment; acceptance criteria

A1.1Process Capability Assessment (Cpk)

Detailed Cpk calculation for solder paste volume (primary CTQ). Formula: **Cpk = min[(USL-mu)/(3*sigma), (mu-LSL)/(3*sigma)]**. Assuming centred process: Cpk = 0.20/(3 x 0.12) = 0.56. This is well below the industry target of 1.33, confirming the process cannot consistently produce within specification. A 57% reduction in sigma is required to achieve Cpk >= 1.33. Source: Montgomery (2019); Becker et al. (2019). See Excel Sheet A1.

Parameter	Value	Source / Interpretation
Specification Limit (USL/LSL)	-0.2	IPC-A-610, acceptable solder paste volume range
Process std deviation (sigma)	-0.12	Becker et al. (2019), published SMT data
Cp (potential capability)	0.56	(0.40)/(6 x 0.12), severely incapable
Cpk (actual capability)	0.56	= Cp (centred process assumed)
Industry minimum Cpk	1	General manufacturing standard process FAILS this
Industry target Cpk	1.33	Montgomery (2019) / IPC-A-610, 4-sigma level
World class Cpk	1.67	Six Sigma convention 5-sigma level
Improvement gap	0.77 Cpk units	1.33 - 0.56 , requires sigma reduction of approx 57%

Table A 1 Table A1.1 Process Capability Summary | Solder Paste Volume CTQ | Excel Sheet A1

Appendix A2 SPC X-bar and R Chart Data (Solder Paste Volume)

This appendix provides the control chart parameters and 20-subgroup dataset for monitoring solder paste volume using Shewhart X-bar and R charts. Subgroup size n=5; constants A2=0.577, D4=2.114, D3=0 per Montgomery (2019).

Chart Parameter	Value	Formula and Interpretation
Subgroup size (n)	5	Standard for SMT solder paste volume monitoring
Grand Mean (X-double-bar)	~100.4% nominal	Average of 20 subgroup means close to 100% target
Average Range (R-bar)	~8.3%	Average within-subgroup variation
UCL (X-bar chart)	~105.2%	X-bar-bar + A2 x R-bar (A2=0.577)
LCL (X-bar chart)	~95.6%	X-bar-bar - A2 x R-bar
UCL (R chart)	~17.5%	D4 x R-bar (D4=2.114, n=5)
LCL (R chart)	0	D3 x R-bar (D3=0 for n<7)
Out-of-control signals	Samples 15 and 18	Upward drift consistent with stencil wear (Section 3.3.1)
Required action	Stencil inspection and replacement	Corroborated by Five Whys root cause analysis

Table A 2 X-bar and R Control Chart Parameters | Full 20-subgroup dataset in Excel Sheet A2

The two out-of-control signals at samples 15 and 18 reflect the progressive stencil wear identified in the Five Whys analysis (Section 3.3.1). In the proposed SPC system (Section 5.2.4), these signals would trigger an automatic machine stop and engineer alert, preventing defective boards advancing to the reflow stage.

Appendix A3 EWMA Chart (Reflow Oven) and P-Chart (AOI)

A3.1 EWMA Control Chart: Reflow Oven Temperature

The EWMA chart (lambda=0.2) is preferred over Shewhart charts for detecting gradual thermal drift in the reflow oven, which is the dominant failure mode for this stage (Section 4.3; Montgomery, 2019). The smoothing parameter lambda=0.2 provides the optimal balance between sensitivity and false-alarm rate for a 1.0-1.5 sigma shift detection target.

Parameter	Value	Justification
Smoothing parameter (lambda)	0.2	Optimal for detecting gradual drift less than 1.5-sigma
Centre Line (target temp)	245 degrees C	Reflow profile specification for SAC305 lead-free alloy
Process sigma	1.2 degrees C	Estimated from published thermal process data
UCL / LCL	245 +/- 3*sigma*sqrt(lambda/(2-lambda))	Montgomery (2019) EWMA limit formula
OOO Signals	Observations 21-25	Downward drift detected oven zone re-calibration required
Advantage vs Shewhart	ARL1 approx 10 vs 43 for 1-sigma shift	Superior sensitivity for small gradual shifts

Table A 3 EWMA Chart Parameters: Reflow Oven Temperature | Excel Sheet A3

A3.2 P-Chart: AOI Proportion Defective per Batch

Parameter	Value	Justification
Batch size (n)	200 boards	Typical SMT batch size for high-volume consumer electronics
Centre line (p-bar)	0.08 (8%)	Based on current 8,500 DPMO performance (approx 8% per batch)
UCL_p	approx 0.137	$p\text{-bar} + 3 \times \sqrt{p\text{-bar} \times (1 - p\text{-bar}) / n}$
LCL_p	approx 0.023	$\max(0, p\text{-bar} - 3 \times \sqrt{p\text{-bar} \times (1 - p\text{-bar}) / n})$
OOB Batches	Batches 8, 15, 23	Above UCL -investigate AOI threshold drift / lighting
Action trigger	Above UCL or 8 consecutive above p-bar	Western Electric Rules adapted for attribute chart

Table A 4 Table A3.2 -P-Chart Parameters: AOI Batch Defect Rate Monitoring | Excel Sheet A3

Appendix A4 KPI Summary Dashboard

The KPI Dashboard consolidates all performance targets across three states: current state baseline, future state post-18-month implementation, and world-class benchmark. Full interactive dashboard with investment vs. return chart available in Excel Sheet A4.

KPI	Current	Future State	World Class	Gap	Priority
OEE (%)	0.72	0.85	>=85%	+13 pp	CRITICAL
DPMO	8500	1500	<3.4 (6-sigma)	-7000	CRITICAL
First-Pass Yield	0.91	0.97	>=99%	+6 pp	HIGH
AOI Cycle Time	25 sec	18 sec	18 sec	-7 sec	HIGH
Changeover Time	47 min	10 min	<10 min	-37 min	HIGH
Total Lead Time	11 hrs	4.5 hrs	<=4 hrs	-6.5 hrs	HIGH
VA Ratio	0.053	>15%	>=25%	+9.7 pp	HIGH
WIP Buffer	4.3 days	1.5 days	<=1 day	-2.8 days	MEDIUM
On-Time Delivery	0.88	0.95	>=97%	+7 pp	MEDIUM
Total CoQ	10.9% rev	6.0% rev	<5% rev	-4.9 pp	CRITICAL
CO2e Reduction	Baseline	-120 tCO2e/yr	Target	-120 tCO2e	LOW

Table A 5 KPI Dashboard: Current vs Future State vs World Class | Excel Sheet A4

Appendix A5 Gauge R and R (MSA) Study Template

A Gauge Repeatability and Reproducibility study must be completed as a mandatory precondition before SPC control limits are set (Section 4.3; Montgomery, 2019). This template is provided for completion using the SPI measurement system. Study design: 3 operators x 10 parts x 2 replicates = 60 measurements. Acceptance criterion: %GRR < 10%. The current SPI system is estimated at 18-22% (MARGINAL), meaning Phase 3 requires measurement system improvement concurrent with control chart deployment.

%GRR Range	Assessment	Required Action
< 10%	ACCEPTABLE	Measurement system adequate - proceed to SPC implementation
10% - 30%	MARGINAL	May be acceptable -review with engineer; document risk
> 30%	UNACCEPTABLE	Do NOT set SPC control limits -fix measurement system first
~18-22% (current SPI estimate)	MARGINAL - action required	Improve SPI calibration and re-validate before Phase 3

Table A 6 GRR Acceptance Criteria | AIAG MSA Manual; Montgomery (2019) | Full template in Excel Sheet A5

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Title:	Peer Review and Individual Effort Factors		
Group:	New Group 7		
Date assessed:	27/03/2026		
Group Member and Student ID	Factor	Feedback	Signature
	$0.90 \leq X \leq 1.10$	<i>Group will need to provide a brief justification for the weighting factors awarded.</i>	
Bindushree Sanjeev Murthy 259045211	1.10	Consistently exceeded expectations; took lead on [e.g., process analysis / quality engineering section]; proactive in coordinating group tasks and ensuring deadlines were met	
Atharva Sudhir Jagtap 259062649	1.0	Contributed equally to group effort; completed assigned sections [e.g., improvement proposals] to a good standard and participated actively in group discussions.	
Ramaswamy Venkatachalapathy 239050556	0.90	Contributed to the project but at a reduced level; engagement with group tasks was inconsistent and output required additional support from other members.	
Gowdham Subramaniyan 259058922	1.0	<i>Fulfilled expected contribution; completed assigned work [e.g., impact assessment] reliably and collaborated effectively within the team.</i>	
Shri Ram Balaji Sundarraj 259061264	1.0	Met expected contribution level; engaged with assigned tasks and supported overall report development.	